

AN12350

LPC802 双 IO 电源供电和电平转换

版本 0 — 2019 年 2 月 20 日

应用笔记

1 引言

LPC802 (TSSOP20) 和 LPC804 (TSSOP24) 配备了新的功能，称为双 I/O 电源芯片。该功能使芯片具有两个电源域：VDDio 和 VDD。封装一侧的引脚由 VDDIO 提供电源，另一侧的引脚由 VDD 提供电源。此功能允许 VDD 和 VDDio 提供不同的电压，使得器件可将信号从一个片外电压域转换至另一个电压域。

目录

1	引言.....	1
1.1	引脚特性.....	1
1.2	引脚比较.....	2
2	有关电平转换的示例.....	2
2.1	示例介绍.....	3
2.2	示例硬件.....	3
2.3	示例软件.....	5
2.4	演示过程.....	5

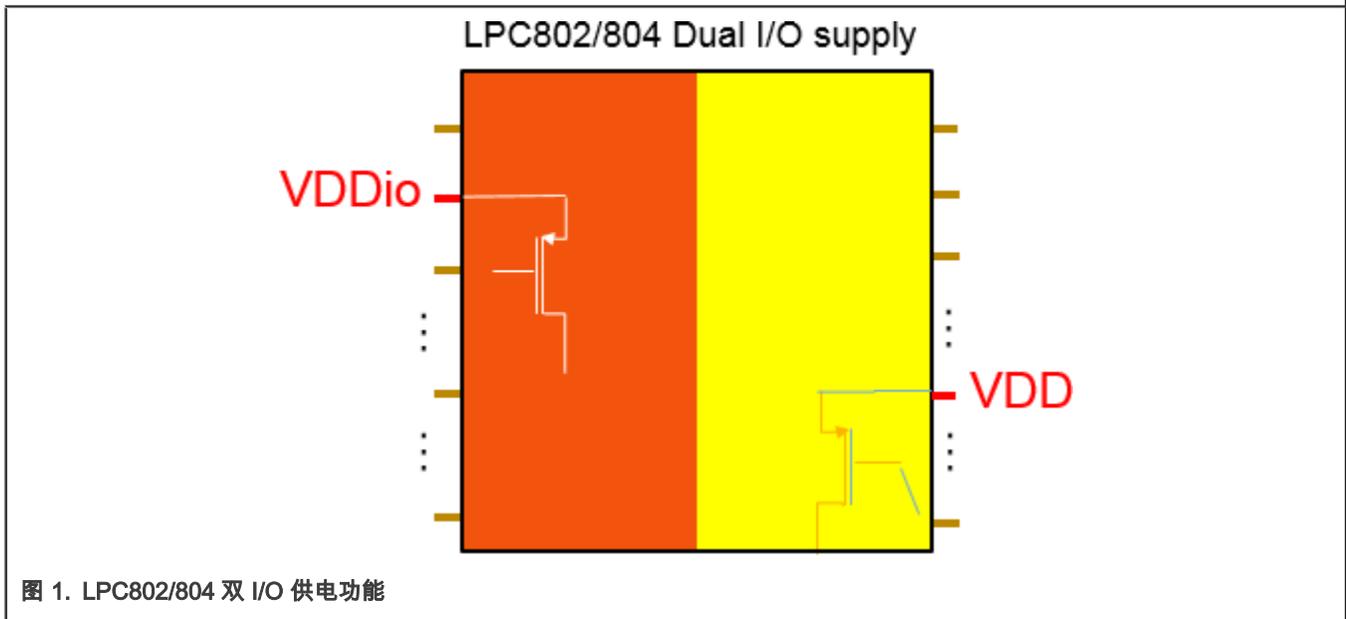


图 1. LPC802/804 双 I/O 供电功能

用户在一个电压域中最多可以选择两个引脚：In0，In1，在另一个电压域中又可以选择两个引脚：Out0，Out1。使用开关矩阵对它们进行路由连接：In0 到 Out0，In1 到 Out1。引脚 In(x)上的一个信号能够直接转移到引脚 Out(x)，而无需任何固件干预，电平就会发生变化。唯一需要做的是：用户定义输入和输出方向。

1.1 引脚特性

双电源功能仅适用于如下特定型号的器件：

- LPC802M011JDH20
- LPC804M111JDH24

相应的引脚电压值和所使用的电源域电压值相一致。

- 对于 VDDio 侧的引脚：



V _O	output voltage	output active		0	-	V _{DDIO}	V
V _{IH}	HIGH-level input voltage			0.7V _{DDIO}	-	-	V
V _{IL}	LOW-level input voltage			-	-	0.3V _{DDIO}	V
V _{hys}	hysteresis voltage			-	0.4	-	V
V _{OH}	HIGH-level output voltage	I _{OH} = 4 mA; 2.5 V ≤ V _{DD} ≤ 3.6 V		V _{DDIO} - 0.4	-	-	V
		I _{OH} = 3 mA; 1.71 V ≤ V _{DD} < 2.5 V		V _{DDIO} - 0.5	-	-	V

图 2. VDDio 侧的引脚规格

- 对于 VDD 侧的引脚：

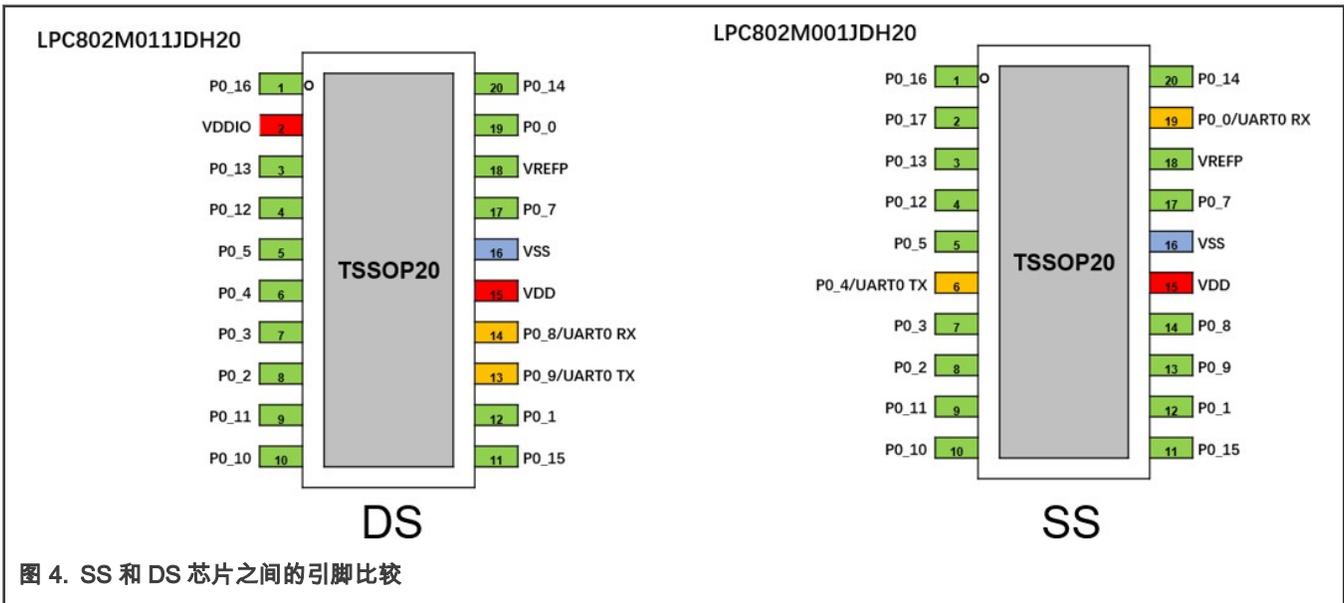
V _O	output voltage	output active		0	-	V _{DD}	V
V _{IH}	HIGH-level input voltage			0.7V _{DD}	-	-	V
V _{IL}	LOW-level input voltage			-	-	0.3V _{DD}	V
V _{hys}	hysteresis voltage			-	0.4	-	V
V _{OH}	HIGH-level output voltage	I _{OH} = 4 mA; 2.5 V ≤ V _{DD} ≤ 3.6 V		V _{DD} - 0.4	-	-	V
		I _{OH} = 3 mA; 1.71 V ≤ V _{DD} < 2.5 V		V _{DD} - 0.5	-	-	V

图 3. VDD 侧的引脚规格

ADC 电源域连接到 VDD 域。对于 ADC 操作，VDD 电压必须高于 2.5 V。

1.2 引脚比较

单电源 (SS) 芯片和双电源 (DS) 芯片分配给引脚的某些功能有所不同，请参阅图 4。



在 DS 芯片中，pin2 用作 VDDio，而在 SS 芯片中，pin2 用作 P0_17 (红色标记的引脚)。

DS/SS 芯片的 ISP USART 引脚分配不同 (引脚标记为黄色)。

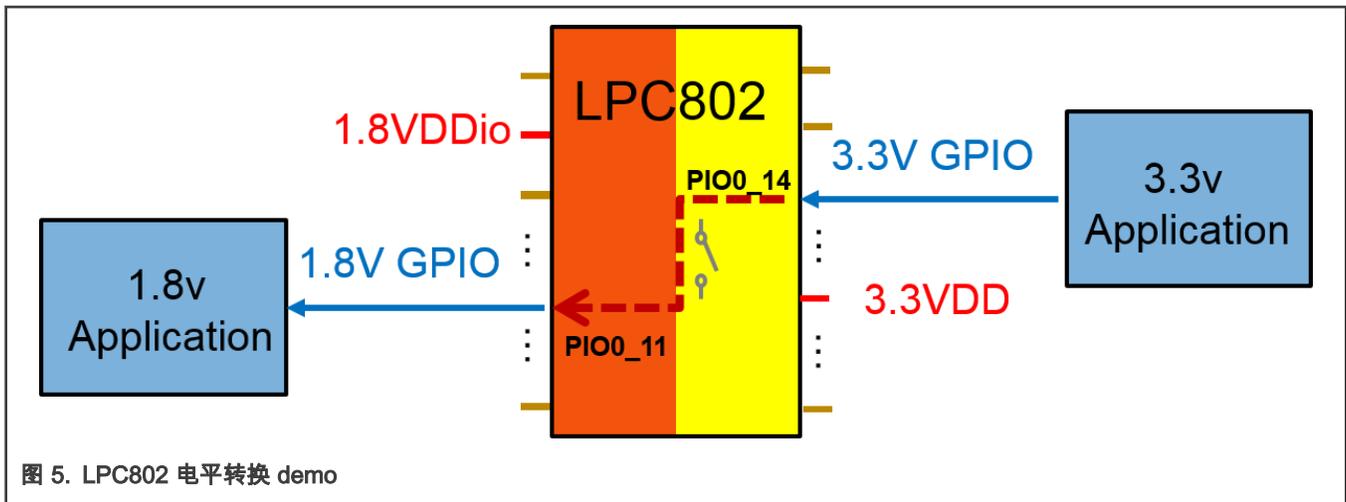
2 有关电平转换的示例

2.1 示例介绍

为了在工作于不同工作电压的应用之间进行通信，需要在它们之间添加一个电平转换芯片。在本示例中，LPC802 用于在两个电压应用之间进行信号电平转换，其中 VDD 侧的 GPIO (PIO0_14) 连接到 3.3 V 应用，而 VDDio 侧的 GPIO (PIO0_11) 连接到 1.8 V 应用。在开始通信之前，LPC802 使用开关矩阵将 PIO0_14 配置为电平转换 input0-In0，将 PIO0_11 配置为电平转换 output0-Out0。配置后，在 In0 上输入的任何 3.3 V 逻辑电平信号都会自动传递到 Out0，且逻辑电平更改为 1.8 V，而无需软件干预。

示例使用 SWM 寄存器 PINASSIGN 6 将 PIO0_14 配置为电平转换 In0，将 PIO0_11 配置为电平转换 Out0。

为了方便在一块板上进行演示，此 demo 使用 GPIO0_9 输出 3.3 V 方波，然后将 PIO0_9 连接到 PIO0_14 (In1)，请参见图 5。



2.2 示例硬件

2.2.1 电路板

LPCXpresso802 开发板 (OM40000)。

2.2.2 调试器

开发板自带的板载调试器，提供 CMSIS-DAP 接口。

2.2.3 电路板设置

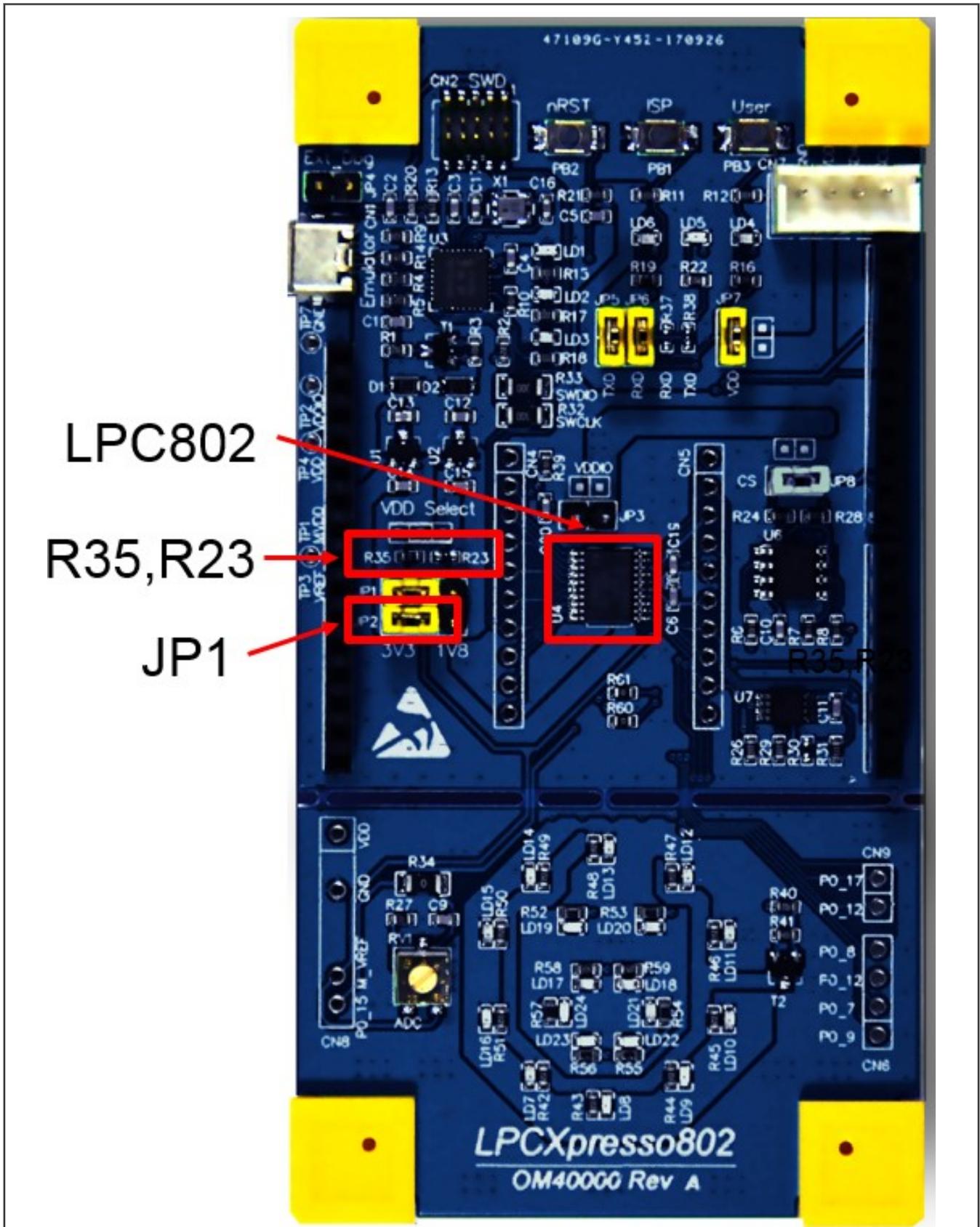


图 6. 电路板设置

- JP1 必须连接到 3.3 V 端，否则 UART 不会输出正确的信息。
- 用 LPC802M011JDH20 (DS 芯片) 替换 LPC802M001JDH20 (SS 芯片)，使芯片具备双 I/O 电源功能。
- 移除 R35，放上 R23 (0 欧姆)，使 VDDIO = 1.8 V。

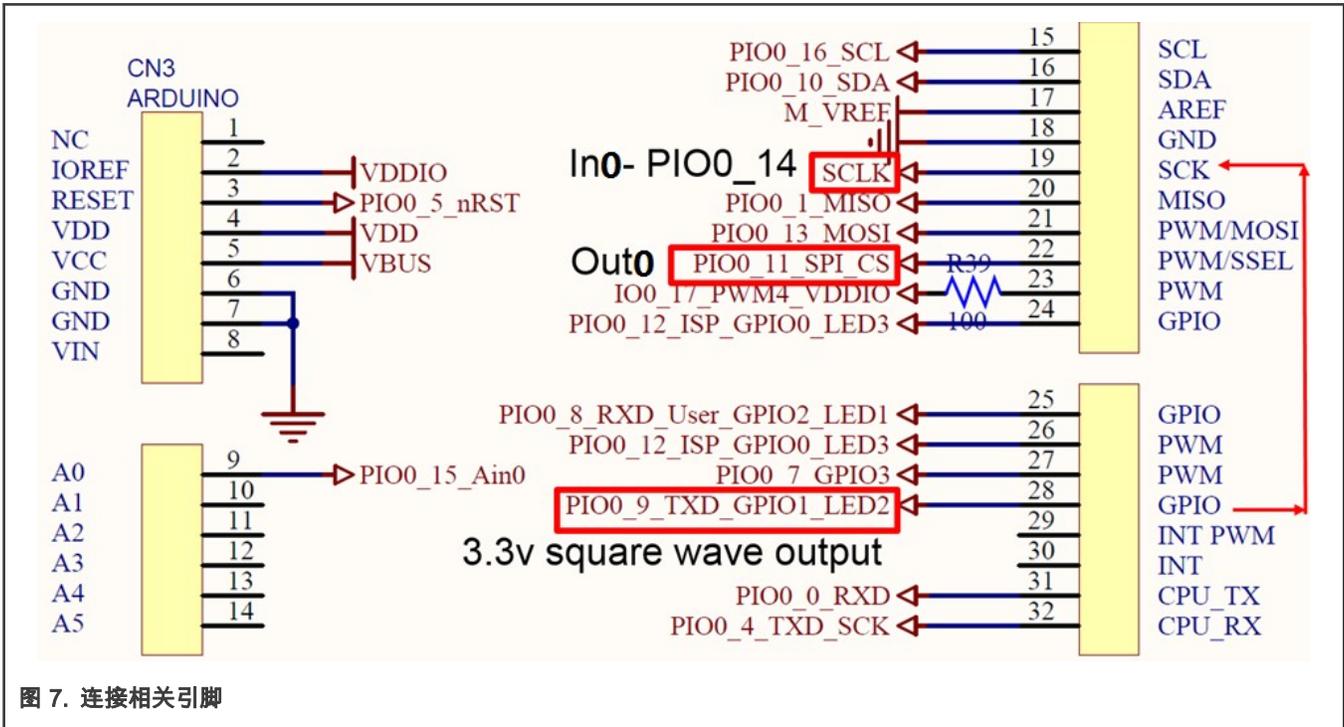


图 7. 连接相关引脚

在 arduino 的端口 CN3 上将 PIO0_9 连接到 PIO0_14。

2.3 示例软件

调试使用的 IDE:

- IAR embedded Workbench 8.22.2
- Keil MDK 5.24a
- MCUXpresso10.2.0

2.4 演示过程

2.4.1 步骤

1. 用 micro USB 电缆连接 PC 主机和 LPCXpresso802 板上 CMSIS DAP 端口 CN1。
2. 在 PC 上打开具有以下设置的串口调试助手 (例如 Tera Term) :
 - 9600 波特率
 - 八个数据位
 - 无奇偶校验位
 - 一位停止位
 - 无流量控制
3. 编译并将代码下载到目标板。
4. 在 IDE 中启动调试器，开始运行相应代码。

5. 在调试控制台上监视信息。
6. 使用示波器观察引脚 PIO0_14_SCLK 上的 3.3 V 输入方波和引脚 PIO0_11 上的 1.8 V 输出方波。

2.4.2 示例结果

运行示例之后，PC 中的串行终端将显示信息，如 图 8 所示。

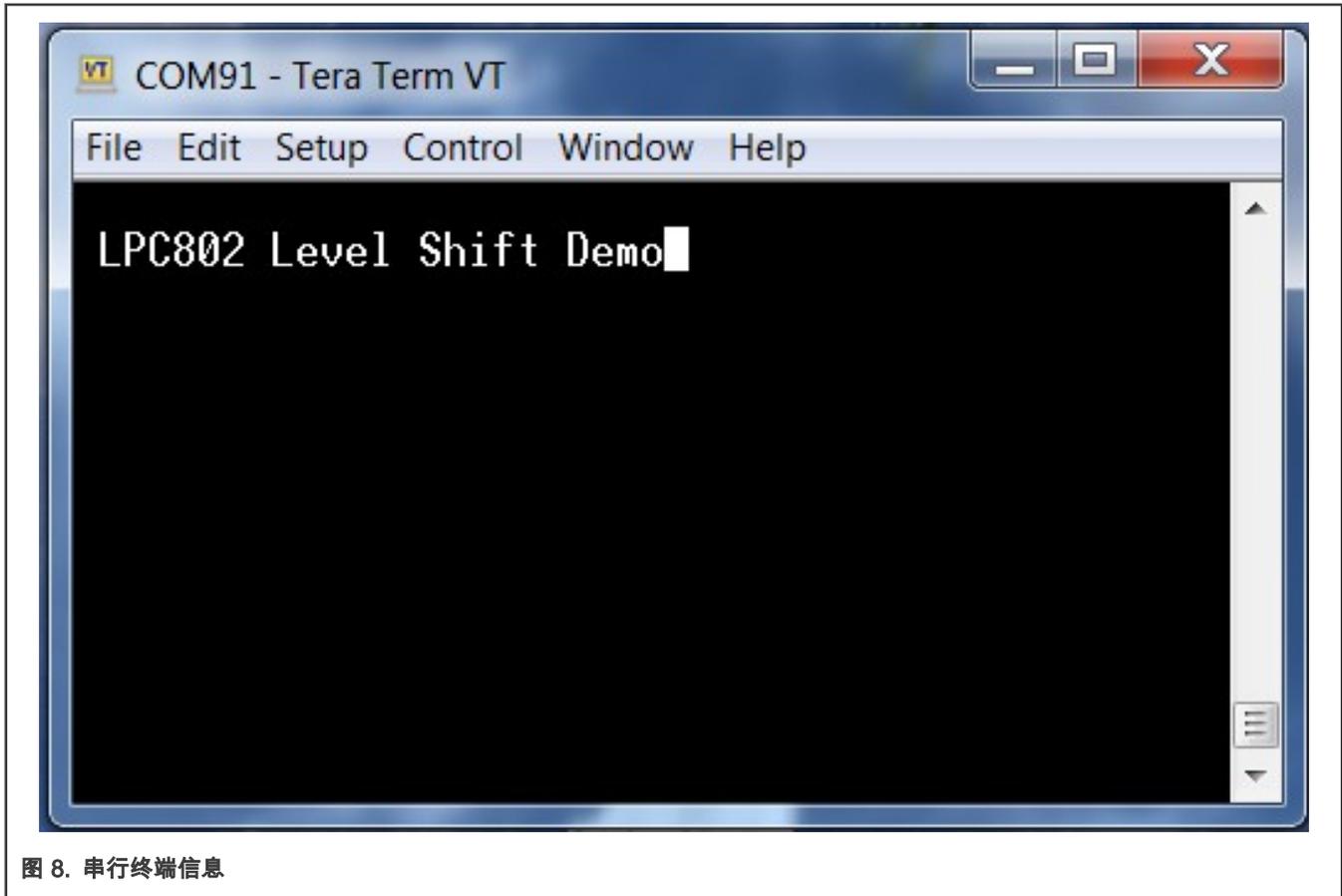


图 8. 串行终端信息

使用示波器观察 PIO0_14_SCLK (VDD 域，电平转换输入) 和 PIO0_11 (VDDio 域，电平转换输出)，可以观察到方波电平从 3.3 V 变为 1.8 V。

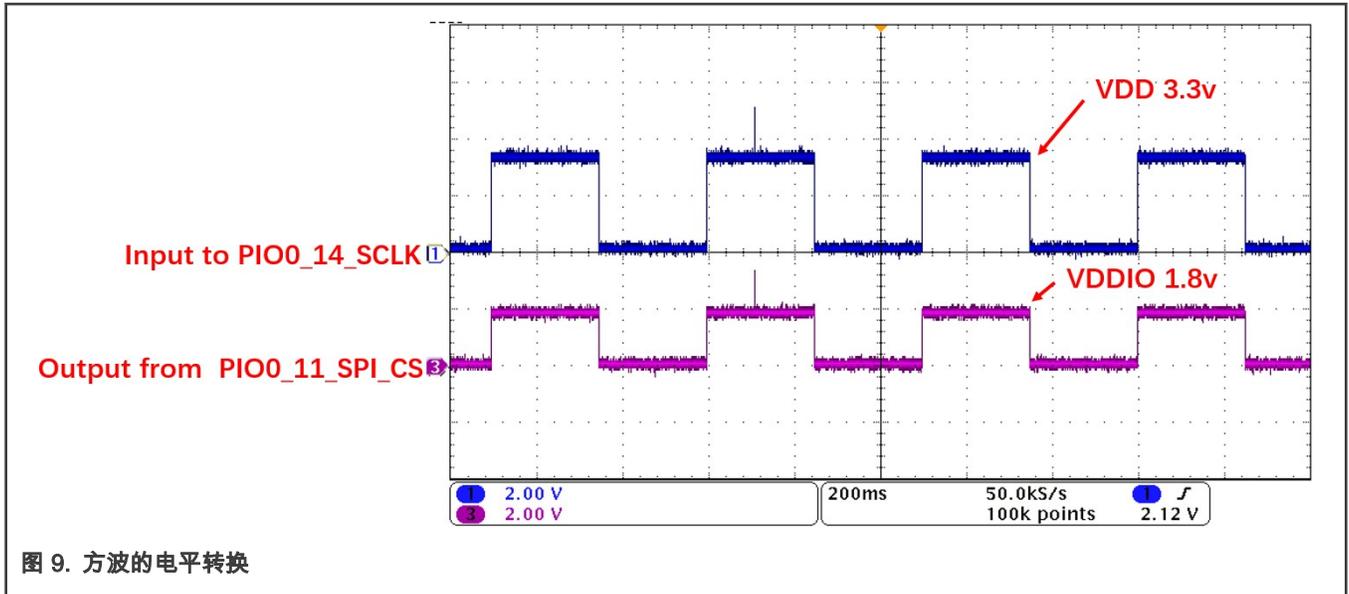


图 9. 方波的电平转换

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Limited warranty and liability — Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

Right to make changes - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer’s applications and products. Customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer’s applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, ICODE, JCOP, LIFE, VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, CodeWarrior, ColdFire, ColdFire+, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, Tower, TurboLink, EdgeScale, EdgeLock, eIQ, and Immersive3D are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, µVision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. M, M Mobileye and other Mobileye trademarks or logos appearing herein are trademarks of Mobileye Vision Technologies Ltd. in the United States, the EU and/or other jurisdictions.

© NXP B.V. 2019-2021.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 2019 年 2 月 20 日

Document identifier: AN12350

